UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/649,958	08/29/2000	Shinji Kimura	ASA-920	7131

24956 7590 01/04/2005

MATTINGLY, STANGER & MALUR, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
PATEL, ASHOKKUMAR B	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/649,958	KIMURA ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the c rresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 9-17 are subject to examination.

Response to Arguments

2. Applicant's arguments with respect to claims 9-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 9-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Blanset et al. (hereinafter Blanset) (US 4, 747, 040)

Referring to claim 9,

The reference teaches a computer system comprising:

a first operating system (OS) (The UNIX ® and MS-DOS ® operating systems are supported in a multi-tasking computer, Abstract, note: considering UNIX ® as being the first operating system)

a multi-OS driver (Fig. 4, Switch .Sys 43,) activated as a device driver of the first OS (col.14, line 58-61, "To this end, in accordance with a feature of the invention, an interrupt assignment table, shown in FIG. 18, is maintained in data area 473 within switch.sys area 45 as well as in the UNIX system kernel.");

a second OS (The UNIX ® and MS-DOS ® operating systems are supported in a multi-tasking computer, Abstract; note: considering MS-DOS ® as being the second operating system); and

a plurality of hardware devices (Fig. 7, elements 130),

wherein the multi-OS driver manages rights of using the hardware devices by the first and second OSs (The UNIX® and MS-DOS® operating systems are supported in a multi-tasking computer. At the heart of the computer is a microprocessor having protected and non-protected modes. The computer includes special-purpose hardware which prevents the MS-DOS system and its applications, which execute in the non-protected mode, from interfering with the UNIX system and its applications, which execute in the protected mode. In particular, this hardware monitors addresses generated by the computer and, by selectively inhibiting the associated control pulses, prevents the MS-DOS system from, for example, writing in UNIX-system-allocated memory, or accessing I/O devices that the UNIX system is currently using.", Abstract),

wherein the multi- OS driver manages notification destinations of interrupts from the plurality of hardware devices to the first and second OSs,

when the first OS uses a first hardware device of the plurality of hardware devices, the first OS notifies the multi-OS driver of a request for use of the first hardware device, wherein the multi- OS driver notifies the first OS of permission for using the first hardware device, if a notification destination of interrupts to an OS received from the first hardware device is not registered as "the second OS" and

wherein the multi-OS driver notifies the first OS of an interrupt from the first hardware device, when receiving the interrupt from the first hardware device after the notification of permission. (col.6, lines 17-32, lines 65 through col. 7, lines 18).

Referring to claim 10,

The reference teaches the computer system according to claim 9, wherein, when the first OS terminates use of the first hardware device, the first OS notifies the multi- OS driver of termination of using the first hardware device, and multi- OS driver deletes information, namely "the first OS'" from a registered notification destination of interrupts to be received from the first hardware device. (col.8, lines 45 through col. 9, line 7)

Referring to claim 11,

The reference teaches the computer system according to claim wherein the multi- OS driver has a management table for managing the notification destinations of interrupts from the plurality of hardware devices (Fig. 18, col.14, line58-61).

Referring to claim 12,

The reference teaches the computer system according to claim 11, further comprising a memory, and wherein the multi- OS driver stored in the memory in an area accessed by the first and second OSs (Fig.4, element switch.sys 43, col.4, lines 36-41, Fig. 18, col.14, line58-61).

Referring to claim 13,

The reference teaches the computer system according to claim 12, wherein the multi-OS driver is mapped in the memory in such a manner that the multi- OS driver is

located in a same address area in both memory space of the first OS and memory space of the second OS (Fig.4 and Fig.5, col.4, lines 11 through col.5, line 8).

Referring to claim 14,

The reference teaches the computer system according to claim 13, wherein, when the first OS loads the multi- OS driver in the memory, the first OS maps the multi- OS driver at an arbitrary address area in the memory space of the first OS, and thereafter, alters mapping in such a manner that the multi- OS driver thus mapped is re-mapped in said same address area (Fig. 18, col.14, line58-61, "an interrupt assignment table, shown in FIG. 18, is maintained in data area 473 within switch.sys area 45 as well as in the UNIX system kernel. That table stores eight bits--one for each of the interrupts I0 to I7. Whenever the UNIX system opens a device for the UNIX (MS-DOS) system, it also sets to "0" ("1") in the interrupt assignment table the bit assigned to the interrupt generated by the device in question, an illustrative assignment of interrupts between the two operating systems being shown in FIG. 18. The interrupt is then said to be "owned" by the UNIX (MS-DOS) system. In accordance with a further feature of the invention, processor 11 is switched to the real (protected) mode whenever an interrupt owned by the MS-DOS (UNIX) system goes off while the processor is in protected (real) mode.")

Referring to claim 15,

The reference teaches the computer system according to claim 14, wherein, the first OS loads the second OS in an area of the memory allocated to the second OS, and activates the second OS, and the second OS maps the same address area. loaded multi- OS driver in said same address area. (Fig.4, 5, col.11, lines 32-49)

Referring to claims 16 and 17,

The reference teaches the computer system according to claim 9, wherein the multi- OS driver notifies the second OS of an occurrence of an interrupt from a second hardware device of the plurality of hardware devices, if a notification destination of interrupts to an OS to be received from the second hardware device is registered as "the second OS"., and the computer system according to claim 16, wherein the multi- OS driver notifies the first OS of no permission for using the second hardware device, when receiving a request for use of the second hardware device from the first OS. (col.6, lines 65 through col. 7, line 18, col.8, line 58 through col.9, line 7)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
***

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100